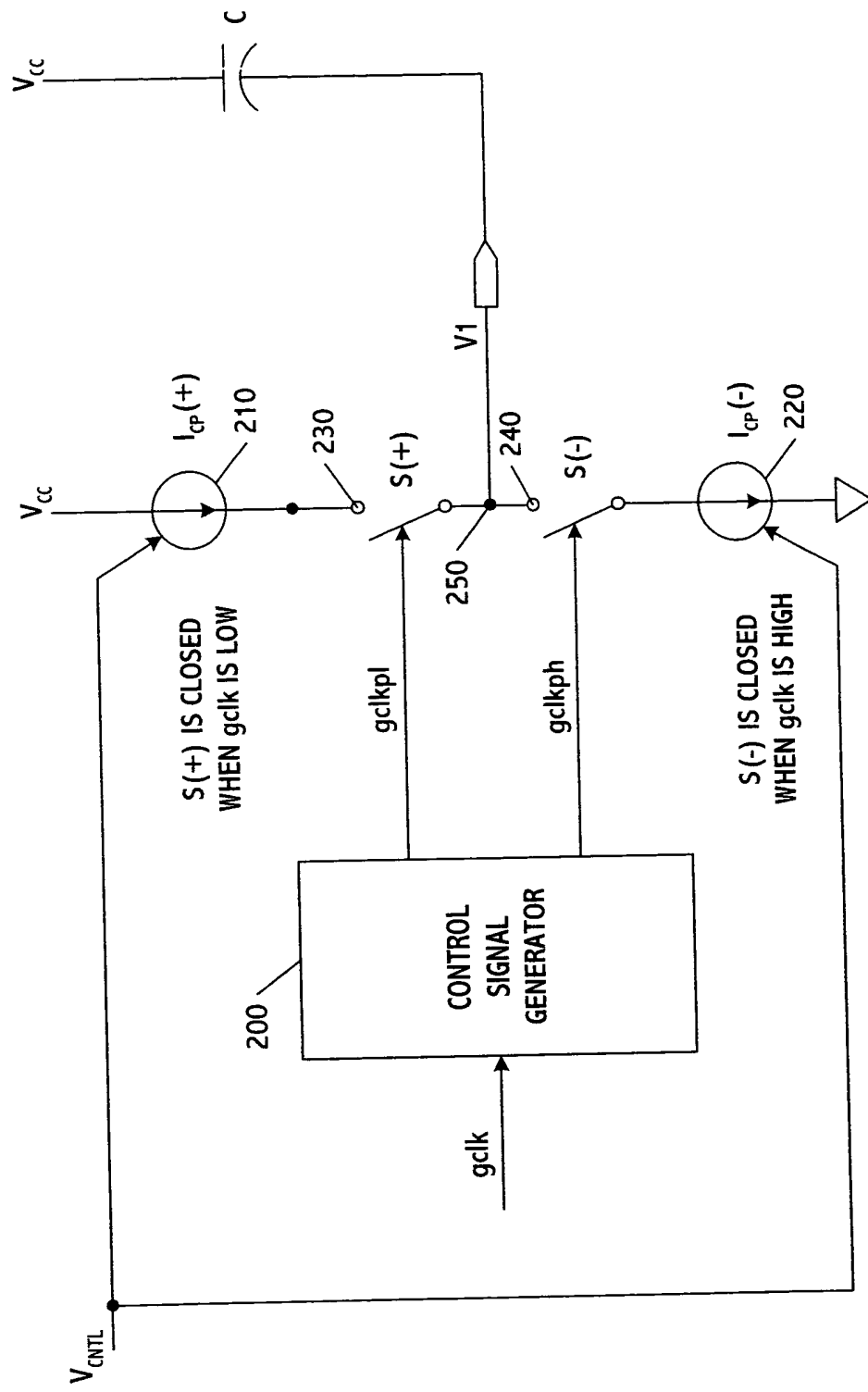
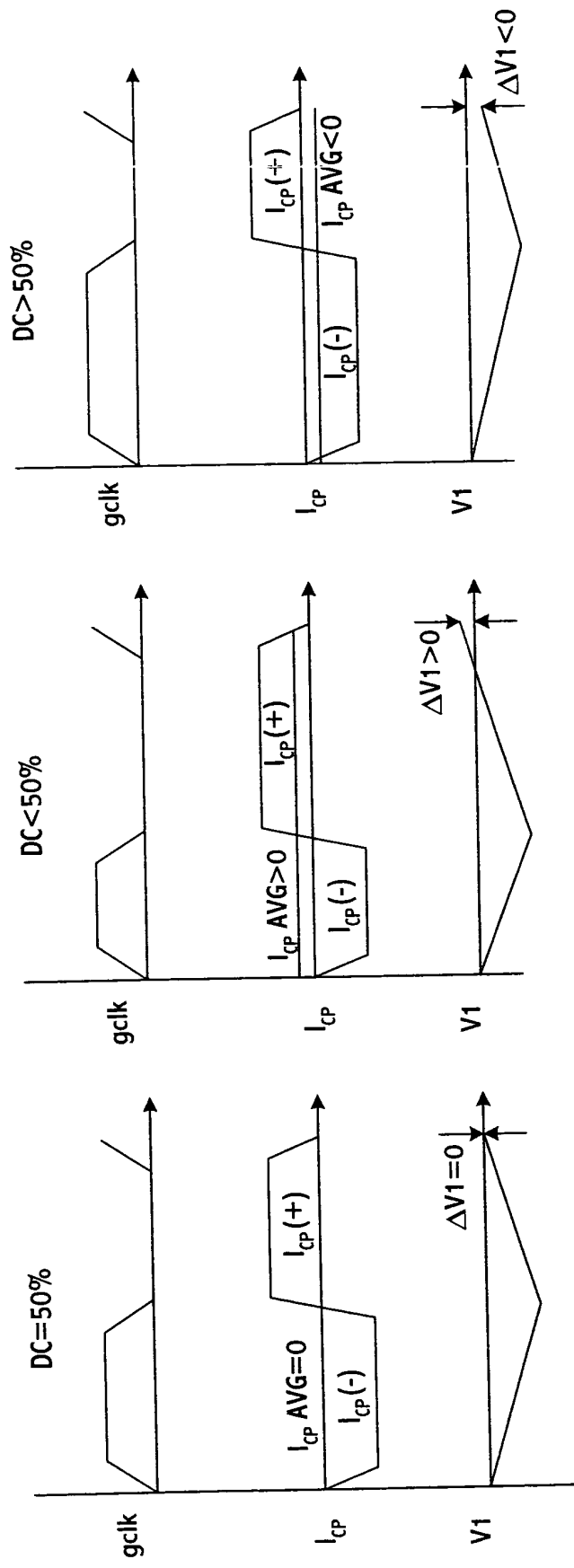


**FIG. 1**



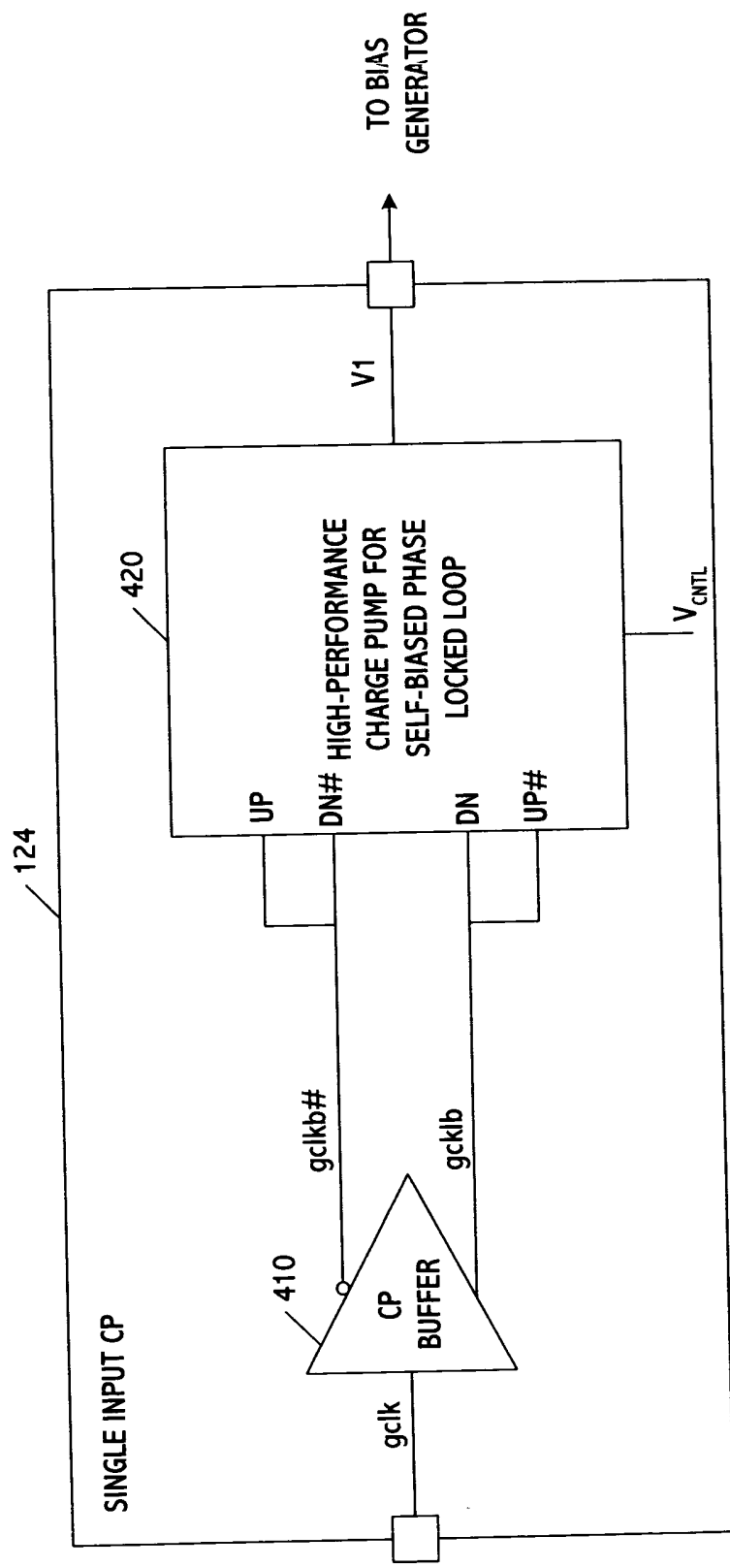
**FIG. 2**



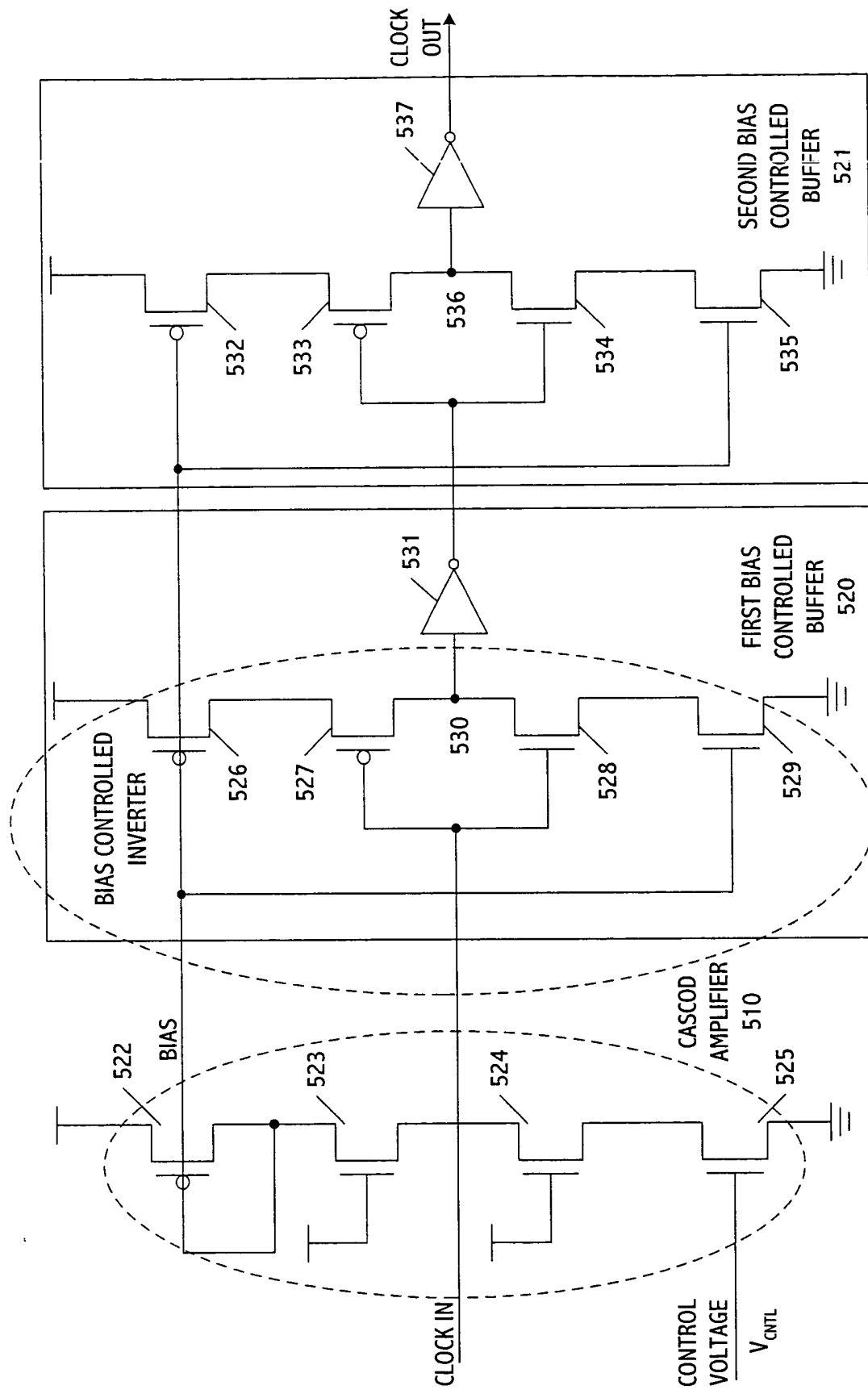
**FIG. 3(a)**

**FIG. 3(b)**

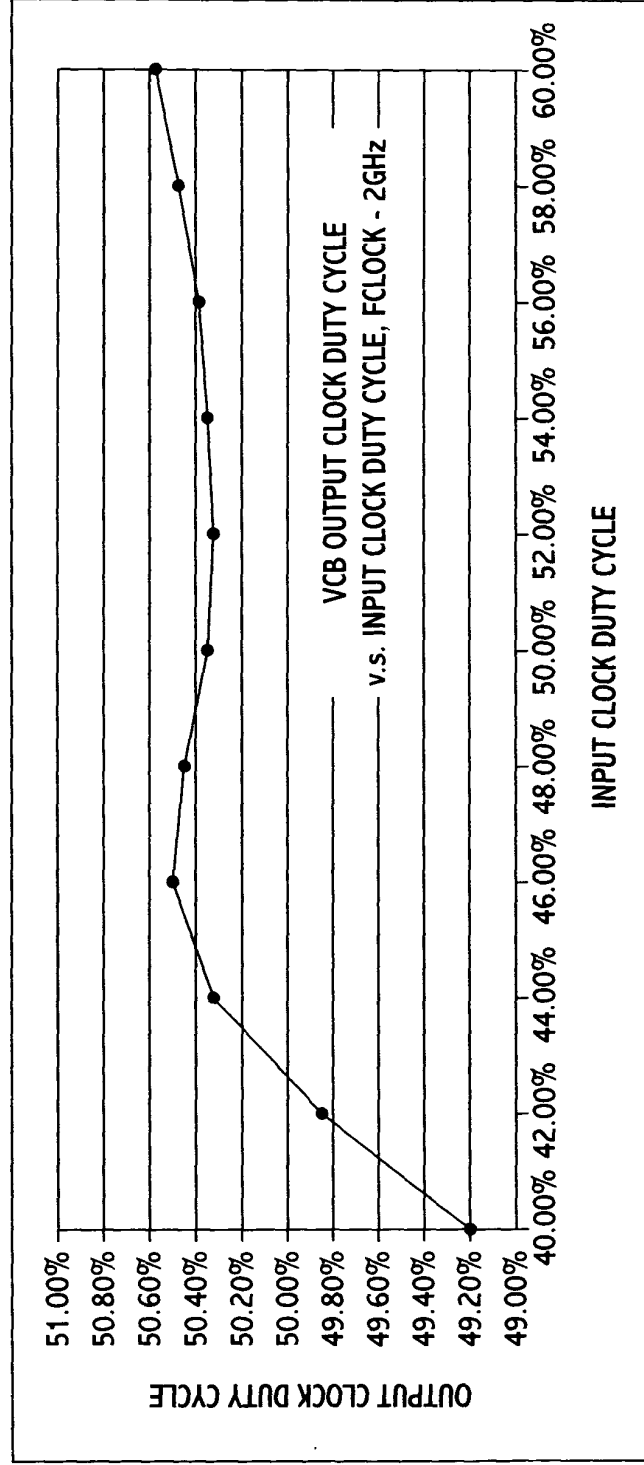
**FIG. 3(c)**



**FIG. 4**

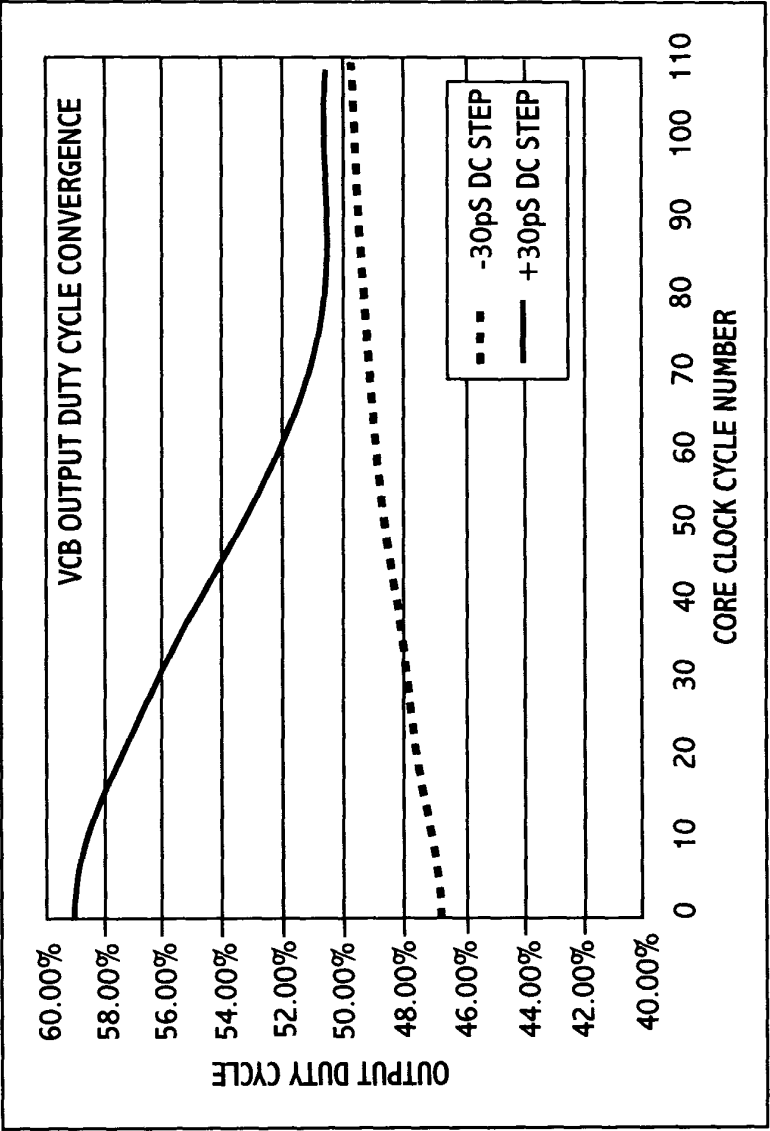


**FIG. 5**



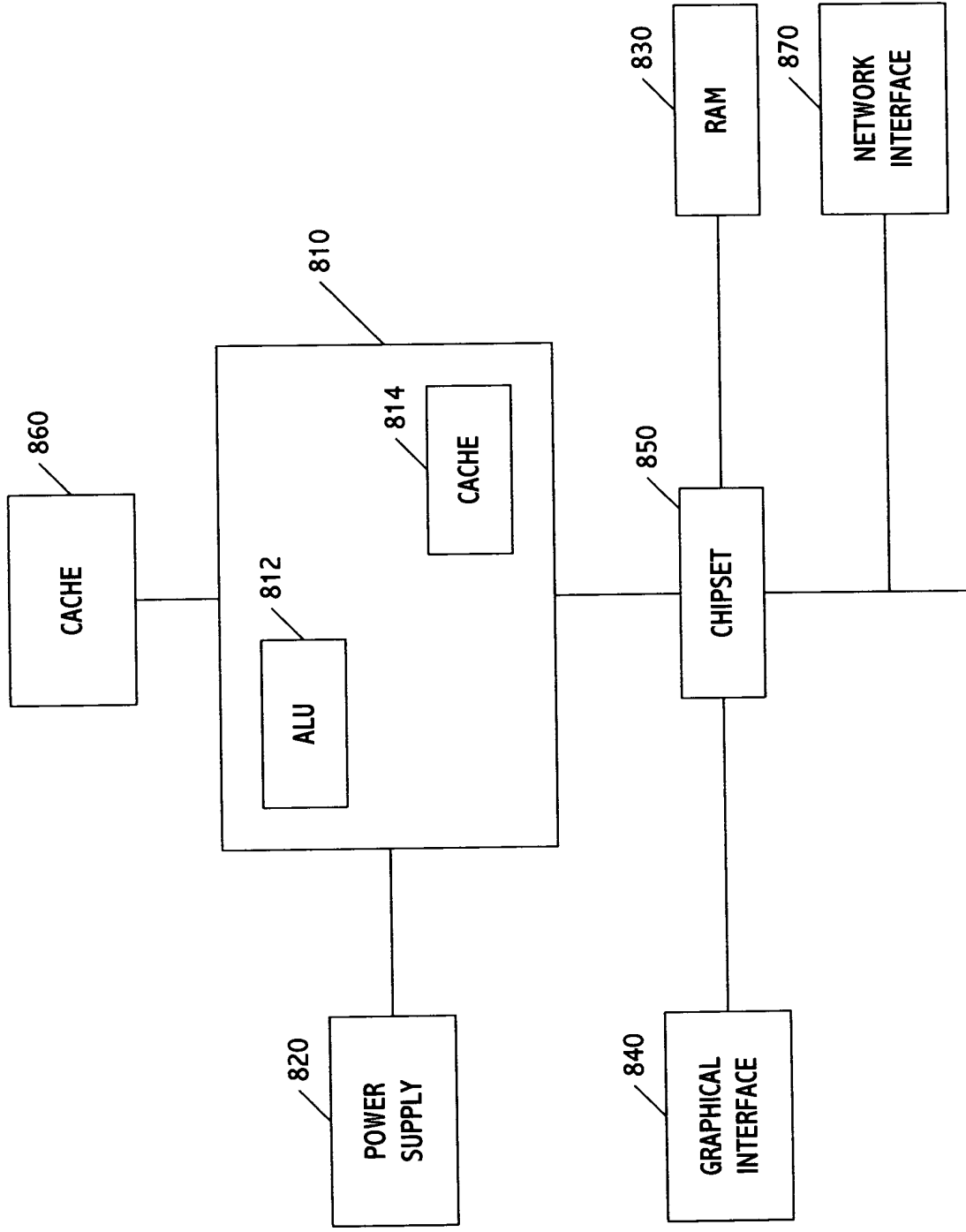
DUTY CYCLE CORRECTION CIRCUIT PERFORMANCE

**FIG. 6**



DUTY CYCLE CIRCUIT CONVERGENCE

FIG. 7



**FIG. 8**